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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,988	09/18/2003	John C. Rudelic	ITL.0602C1US (P11743C)	6661

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Timothy N. Trop
TROP, PRUNER & HU, P.C.
STE 100
8554 KATY FWY,
HOUSTON, TX 77024-1805

EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 06/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,988	RUDELIC ET AL.	
	Examiner	Art Unit	
	Michael t Tran	2818	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-16 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7,8 and 13-16* is/are rejected.

7)☒ Claim(s) *4-6,10-12 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated May 20, 2004, claims 1-8, 10-16, and 18-20 are active in this application.

Claim Objections

2. Claims 4-6, 10-12, and 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections – 35 U.S.C. § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 1-3 are rejected under 35 U.S.C 102(b) as being anticipated by Korsh et

al. [U.S. Patent #6,396,742].

With respect to claim 1, Korsh et al. disclose, in column 25, lines 30-45, a method comprising: storing data at a first density in a first cell in a first memory; and storing data at a second density in a second cell in the first memory. In the cited section, Korsh et al. indicated that a multilevel storage system can store a different number of bits per cell in different portion of an array.

With respect to claim 2, Korsh et al. disclose a method wherein storing data at a second density in a second cell includes storing fewer bits per cell in one of said first or second cells. As stated above, in the cited section, Korsh et al. indicated that different memory cells within an array of memory cells can be programmed to store different densities. See column 25, lines 30-45.

With respect to claim 3, Korsh et al. disclose the method of changing the number of bits per cell dynamically. See column 21, lines 25-34.

5. Claims 7-8 are rejected under 35 U.S.C 102(b) as being anticipated by Korsh et al. [U.S. Patent #6,396,742].

With respect to claim 7, Korsh et al. disclose an article comprising a medium storing instructions, that, if executed, enable a processor-based system to: store data at a first density in a first cell in a first memory; store data at a second density in a second cell in said first memory array; and dynamically change the number of bits stored per cell. In the column 25, lines 30-45, Korsh et al. indicated that a multilevel storage system can store a different number of bits per cell in different portion of an array.

Korsh et al. further state that changing the number of bits per cell can also improve read and write speeds.

With respect to claim 8, Korsh et al. disclose a method wherein storing fewer bits per cell in one of said first or second cells. As stated above, in the cited section, Korsh et al. indicated that different memory cells within an array of memory cells can be programmed to store different densities. See column 25, lines 30-45.

6. Claims 13-16 are rejected under 35 U.S.C 102(b) as being anticipated by Korsh et al. [U.S. Patent #6,396,742].

With respect to claim 13, Korsh et al. disclose a memory comprising: a memory array including a first and second cell; and a controller coupled to said array to store data in said array at a first density in the first cell and to store data at a second density in the second cell wherein said controller to dynamically change the number of bits stored per cell. In the column 25, lines 30-45, Korsh et al. indicated that a multilevel storage system can store a different number of bits per cell in different portion of an array. Korsh et al. further state that changing the number of bits per cell can also improve read and write speeds.

With respect to claim 14, Korsh et al. disclose, in column 1, that the device directs to a nonvolatile memory device – a flash memory is nonvolatile.

With respect to claim 15, Korsh et al. disclose, in column 1, that the device relates to a multilevel nonvolatile memory.

With respect to claim 16, Korsh et al. disclose a method wherein storing fewer bits per cell in one of said first or second cells. As stated above, in the cited section, Korsh et al. indicated that different memory cells within an array of memory cells can be programmed to store different densities. See column 25, lines 30-45.

Allowable Subject Matter

7. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- Including storing data at levels which are spaced from one another in said cell in order to improve the read fidelity.
- Storing data in regularly spaced levels within a cell while leaving intervening levels within the cell unoccupied by stored data.

Conclusion

8. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

9. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

10. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2818
June 17, 2004